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T-VEC Tester for Simulink and Stateflow Training Course

Course Overview

This course uses lecture and exercises to discuss the motivation, concepts, implementation and usage of the T-VEC Tester for Simulink and Stateflow-based models that supports automated model analysis, model-based test generation, test driver generation, test execution and results analysis. The course will cover topics that will help attendees learn to:

- Analyze Simulink models for unsatisfiable conditions and model defects
- Generate test vectors from Simulink models
- Generate test drivers to execute tests against code generated with the Real-Time Workshop and MATLAB Simulator
- Customize test driver generation for target testing environments
- Verify dynamic behavior in Simulink and on the target using test sequences
- Prove properties about Simulink models

The integrated environment generically referred to as the Test Automation Framework (TAF) integrates commercially available model development and test generation tools. TAF integrates the DOORS® requirement management tool with the T-VEC Tabular Modeler (TTM) for requirement modeling. DOORS integrates also with Simulink/Stateflow®, which supports design-based models. TAF integrates requirement models with design models to provide full traceability from the requirements source to the generated tests, as reflected in Figure 1.Finally, TAF integrates with code coverage tools such as LDRA and VectorCAST too.

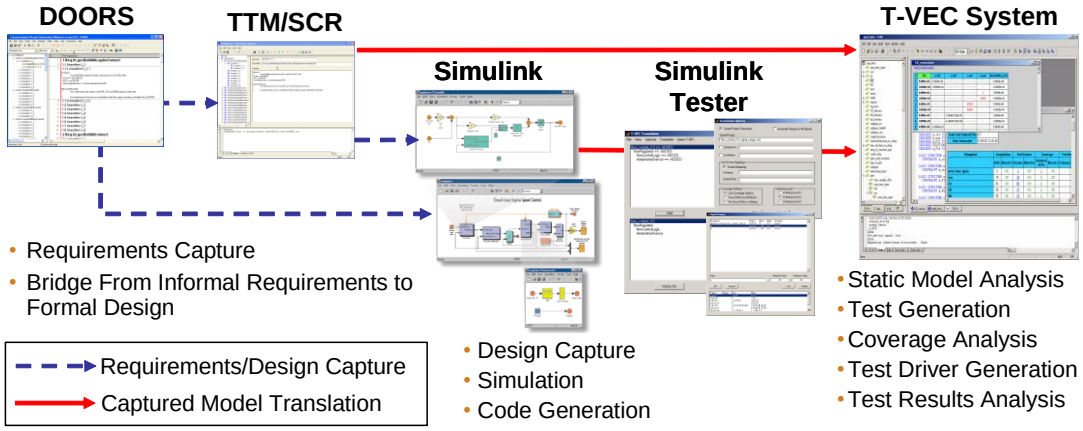

Figure 1. Modeling Tool Chain and Integrated Environment

The course provides attendees with general concepts about how Simulink models can be translated, so that test vectors can be systematically generated to cover all of the paths associated with the code that is generated from the model. The course uses exercises that lead attendees through the process of model translations, test generation, code generation, test driver generation, test execution, and test results analysis. Even though the course leads people through the steps so that they can understand the process, the translator also produces a make file. By executing the make file, it will perform all of the steps automatically (if the model does not have any contradictions). Test vectors can also be executed against the MATLAB simulator (as well as generated code). Test sequences can also be generated automatically with test drivers to run against generated code or the MATLAB simulator. The course also provides attendees with details usage guidelines for the T-VEC tools including the Graphical User and Console interfaces.

The TAF/T-VEC approach leverages Simulink/Stateflow models to automate many traditionally manual and error-prone testing activities by combining commercially-available model-based development, analysis and testing tools. It promotes a continuous V&V process during development providing Simulink model developer model analysis and test generation capabilities during development, thus eliminating the time consuming activity of developing test cases to assess their models.

Learning Objectives: Upon completion of this course, attendees will be able to:

- Introduction to Simulink test automation
- Tool installation and usage overview
- Model translations user interface, configurations and options
- Signal range definition and usage
- Test generation overview
- Test execution overview
- Results analysis overview
- Conclude test automation details
- Test generation of hierarchical models
- Model analysis
- Test driver concepts
- Verifying dynamic behavior using test sequences
- Using assertions to verify model properties
- Guidelines for model development
- Stateflow
- Advanced topics
- Discussion of evolution, needs and support

Resources

If possible, course attendees should bring a laptop with the following minimum configuration: Windows XP, or Windows 7 with at least 1GB RAM (recommended) and a 1GHz processor.

Who Should Attend

The intended audience for this course includes software or system engineers, Simulink developers, and Test engineers.

Contact Us about Training:

Maureen Murtha
E-mail: maureen@knowledgebytes.net
Phone: 703.999.2734